VFE-100 front-end card

VFE-100 is a front-end card for the ZCU111 evaluation kit of the 1st generation Zynq Ultrascale+ RFSoC by AMD Xilinx.

The VFE-100 provides AC-coupled, single-ended, 50 ohm impedance connections to all eight ADC and DAC channels with SMA connectors. An additional on-board DAC can be used to provide a DC bias offset to each output port individually, added through a bias tee. It also provides buffered input and output digital / trigger signals.

Digital / trigger ports

Name	VFE-100 port	XM500 schematic name	ZCU111 FPGA pin	FPGA direction
Trigger input 1	TI1	ADCIO_00	AP5	In
Trigger input 2	TI2	ADCIO_02	AR6	In
Trigger input 3	TI3	ADCIO_05	AU7	In
Trigger input 4	TI4	ADCIO_07	AU8	In
Trigger output 1	TO1	ADCIO_04	AV7	Out
Trigger output 2	TO2	ADCIO_01	AP6	Out
Trigger output 3	TO3	ADCIO_06	AV8	Out
Trigger output 4	TO4	ADCIO_03	AR7	Out

Trigger input and output ports are buffered by SN74LVC1T45 bus transceivers.

ADC / DAC pinout and trace lengths

Name	VFE-100 port	Trace length* (mm)
RFMC_ADC_00	IN1	92.85
RFMC_ADC_01	IN2	92.85
RFMC_ADC_02	IN3	70.38
RFMC_ADC_03	IN4	70.39
RFMC_ADC_04	IN5	47.23
RFMC_ADC_05	IN6	47.23
RFMC_ADC_06	IN7	55.49
RFMC_ADC_07	IN8	55.41
RFMC_DAC_00	OUT1	40.35
RFMC_DAC_01	OUT2	36.73
RFMC_DAC_02	OUT3	53.72
RFMC_DAC_03	OUT4	53.72
RFMC_DAC_04	OUT5	79.43
RFMC_DAC_05	OUT6	79.40
RFMC_DAC_06	OUT7	103.83
RFMC_DAC_07	OUT8	103.88

* trace length from pin on board-to-board connector to transformer (differential). In addition all ADC traces have 12.05 mm from transformer to SMA connector (single ended); all DAC traces have 5.68 mm from transformer to bias tee (single ended) and 9.77 mm from bias tee to SMA connector.

BIAS DAC control

Name	VFE-100 port	XM500 schematic name	ZCU111 FPGA pin	FPGA direction
BIAS DAC SCLK	N/A	DACIO_00	A9	Out
BIAS DAC SDO	N/A	DACIO_01	A10	In
BIAS DAC *CS	N/A	DACIO_02	A6	Out
BIAS DAC SDI	N/A	DACIO_03	A7	Out
BIAS V- ENABLE	N/A	DACIO_04	A5	Out

BIAS V- ENABLE

When DAC80508M is powered by 3.3V the startup output voltage is 0 which would output max negative bias voltage. To prevent this, the negative power supply is disabled on startup and can be enabled by asserting the signal ”BIAS V- ENABLE” once the converter has been properly initialized.

BIAS DAC output mapping

Each output port on VFE-100 has a bias-tee connected to one output of the BIAS DAC (Texas Instruments DAC80508M) as per the table below (note “reverse” order).

VFE-100 port	DAC8050M pin	DAC80508M name
OUT1	11	OUT7
OUT2	10	OUT6
OUT3	9	OUT5
OUT4	8	OUT4
OUT5	5	OUT3
OUT6	4	OUT2
OUT7	3	OUT1
OUT8	2	OUT0

BIAS DAC example VHDL code

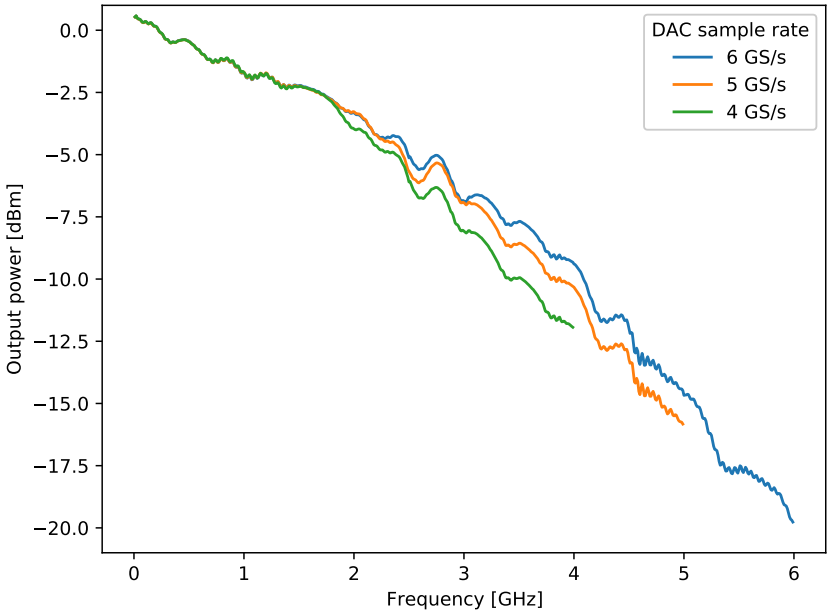
The following code is provided as an example on how to program the DAC80508M from the FPGA. The code is provided ”as is”, without warranty of any kind.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity dac_writer is
    port (
        clk   : in  std_logic;
        reset : in  std_logic;
        data  : in  std_logic_vector(23 downto 0);
        sclk  : out std_logic := '0';
        sdi   : out std_logic := '0';
        csm   : out std_logic := '1'
        );
end dac_writer;

architecture rtl of dac_writer is
    signal shift_reg : std_logic_vector(23 downto 0) := (others => '0');
    signal state     : std_logic_vector(1 downto 0)  := "00";
    signal my_sclk   : std_logic                     := '1';
begin
    process (clk)
        variable count : unsigned(5 downto 0) := (others => '0');
    begin
        if rising_edge(clk) then
            if reset = '1' then
                sclk      <= '0';
                sdi       <= '0';
                csm       <= '1';
                my_sclk   <= '1';
                shift_reg <= data;
                state     <= "01";
                count     := (others => '0');
            else
                my_sclk <= (not my_sclk);
                if state = "01" then     -- init
                    if count = (23 * 2 + 1) then
                        state <= "00";
                    end if;
                    csm   <= '0';
                    sdi   <= shift_reg(23 - to_integer(count(5 downto 1)));
                    sclk  <= my_sclk;
                    count := count + 1;
                elsif state = "00" then  -- idle
                    csm  <= '1';
                    sdi  <= '0';
                    sclk <= '0';
                end if;
            end if;
        end if;
    end process;

end rtl;
```

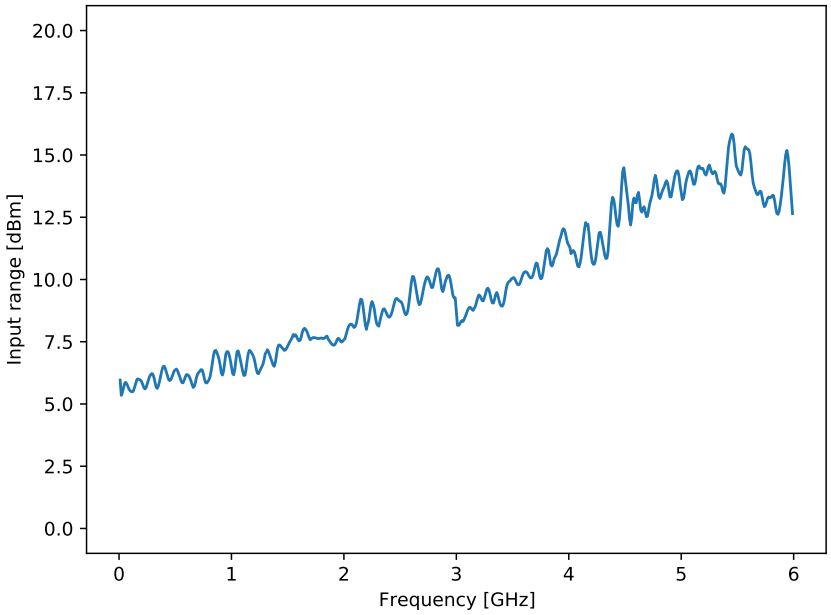
Performance characteristics

Output power range

Typical full-scale output power for different ZCU111 DAC sample rates.

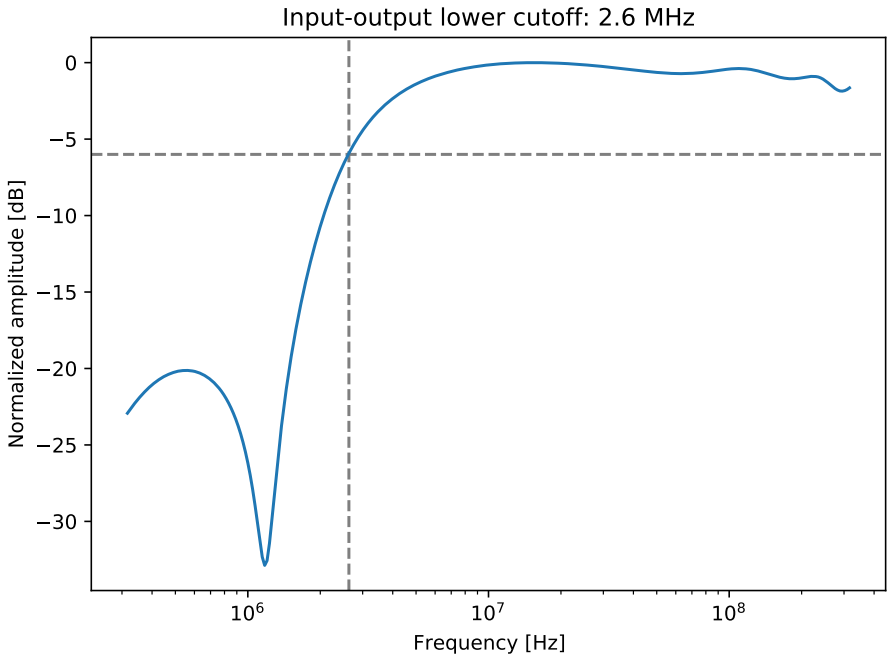


Input power range



Input level which would saturate the ZCU111 ADC. Extrapolated from measurement at -2.5 dBm.

Low-frequency response



Measured in loop-back.

Digital markers / triggers

Output rise time, 10-90%	670 ps
Output rise time, 20-80%	440 ps
Output fall time, 90-10%	570 ps
Output fall time, 80-20%	360 ps

Hardware revisions

Revision number in silk screen below logo.

2022-05: SMA connectors changed. No significant effect on performance. No user action required.

2019-12: Original revision.